REMARKS

Claim 14 has been cancelled. Thus, claims 1-13 and 15-57 are pending in the present application. In the Office Action, claim 14 was rejected under 35 U.S.C. 101 as being a substantial duplicate of claim 12. Claim 14 has been cancelled, rendering the Examiner's rejection moot.

In the Office Action, claims 3, 9, and 21 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 3, 9, and 21 have been amended and Applicant respectfully requests that the Examiner's rejections of claims 3, 9, and 21 under 35 U.S.C. § 112, second paragraph, be withdrawn.

In the Office Action, claims 1-2, 4-8, 10-15, and 30-57 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Moriarty, et al (U.S. Patent No. 6,446,149). Claims 1-2, 4-8, 10-15, 30-31, and 47-48 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Parks (U.S. Patent No. 6,356,983). Claims 1-2, 4-8, 10-15, and 30-57 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Scholhamer, et al (U.S. Patent No. 6,636,921). Claims 16-18 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Moriarty in view of Kao, et al (U.S. Patent No. 6,651,168). Claim 14 has been canceled, rendering the Examiner's rejections of this claim moot. The Examiner's remaining rejections are respectfully traversed.

With regard to independent claims 1, 7, 18, 30, 41-42, and 47, Applicants describe and claim setting and storing a master mode bit. Setting the master mode bit in a master mode register of each of one or more bus interface logics or other devices that include the master mode register is used to establish a secure transmission channel between the master mode logic and the

data input device, *i.e.* setting the master mode bit is used to place the one or more bus interface logics in a master mode. See Patent Application, page 94, ll. 7-10. In the master mode, the master mode logic and the data input device exchange data outside the operating system of the computer system through the bus interface logics or other devices that include the master mode register. As defined in the specification, the phrase "operating outside the operating system" means that programs running under the operating system are unable to access the bus interface logics or other devices including a master mode register when the master mode bit is set. This may advantageously allow for a program running under the operating system to request the crypto-processor or other master device including the master mode logic to perform a secure data read. See Patent Application, page 95, line 23 - page 96, line 2.

The Examiner cites several references (Moriarty, Parks, Scholhamer, and Kao) that describe limiting access to one or more portions of the computer system based upon information stored in a memory. For example, Moriarty describes allowing exclusive access by a busmaster to a shared critical resource based upon the contents of a semaphore memory cell. However, none of the references cited by the Examiner describe or suggest a master mode bit, *i.e.* a bit that indicates that one or more bus interface logics or other devices will be used to establish a secure transmission channel between a master mode logic and a data input device while operating outside the operating system. For at least this reason, Applicants respectfully submit that claims 1-2, 4-8, 10-15, and 30-57 are not anticipated by any of the cited references and request that the Examiner's rejections of these claims under 35 U.S.C. 102(e) be withdrawn.

Moreover, it is respectfully submitted that the pending claims are not obvious in view of the cited references, either alone or in combination. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the

claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). As discussed above, Applicants respectfully submit that the cited references, either alone or in combination, failed to teach or suggest a master mode bit, *i.e.* a bit that indicates that one or more bus interface logics or other devices will be used to establish a secure transmission channel between a master mode logic and a data input device while operating outside the operating system. For at least this reason, Applicants respectfully submit that the present invention is not obvious over the cited references, either alone or in combination, and request that the Examiner's rejections of claims 16-18 under 35 U.S.C. 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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